

UNITED STATES PATENT APPLICATION

FOR

ENCAPSULATION METHOD AND LEADFRAME FOR LEADLESS
SEMICONDUCTOR PACKAGES

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ENCAPSULATION METHOD AND LEADFRAME FOR LEADLESS
SEMICONDUCTOR PACKAGES

CROSS-REFERENCE TO RELATED APPLICATIONS

[0001] This is a divisional of Application Number 10/113,526 Filed March 28, 2002.

FIELD OF THE INVENTION

[0002] The present invention relates to an encapsulation method and leadframe for semiconductor packages and, more particularly, to an encapsulation method and leadframe for leadless semiconductor packages.

BACKGROUND OF THE INVENTION

[0003] Conventional encapsulation methods for packaging semiconductor devices are classified into two kinds. The first encapsulation method is applied to semiconductor packages with leads, as shown in Fig. 1. A plurality of dice are respectively mounted in cavities 11 of a leadframe 1, and are connected to the pins of the leadframe 1. The leadframe 1 has runner 12, and the runner 12 is connected to the cavities 11 by sub-runners 13 and gates 14. Each gate 14 is an injection inlet between a sub-runner 13 and a cavity 11. Molding material is injected into the runner 12 and moves via the sub-runners 13 and the gates 14 to cavities 11 so as to package the dice in cavities 11. This encapsulation method requires space for the runner 12 and the sub-runners 13, thereby decreasing the number of dice within the leadframe area, and does not have high packaging efficiency.

[0004] The second encapsulation method is applied to leadless semiconductor packages, as shown in Fig. 2. A plurality of dice 22 are placed in a cavity 21. Molding material is injected into the cavity 21 to package the dice 22. Therefore, the number of dice within the leadframe is increased, and the cost of the leadframe can be decreased. However, the second method must use cutting equipment to cut the packaged semiconductor devices into individual pieces, and the cutting equipment is usually expensive. Therefore, the cost of the second method is high. Furthermore, after the semiconductor devices are cut, every one of the semiconductor devices must be transferred to a tray or a tube so that the steps of the second method are complex and the efficiency of the second method is low.

[0005] Besides, as shown in Fig. 3, each packaged semiconductor device 3 has no contact leads. Instead, device 3 has a plurality of conducting portions 31 for connection to a circuit board. When the leadless semiconductor device 3 is packaged, molding flash must not remain on the conducting portions 31. Therefore, during the packaging process, a film at the bottom of the semiconductor device 3 is needed to prevent molding flash from remaining on the conducting portions 31. Such a film increases the cost of the second method and degrades the efficiency.

[0006] On the other hand, the second method must utilize an upper mold and a lower mold to clamp the periphery of the leadframe 2, and the molding material is injected into the cavity 21 formed by the upper and lower molds. Because the cavity 21 is large, the upper and lower molds can only clamp the periphery of the lead frame 2. The middle portion of the

cavity 21 cannot be clamped by the upper and lower molds. This will easily cause molding flash to remain on the conducting portions 31.

[0007] Therefore, it is desirable to provide a creative and improved encapsulation method and leadframe to overcome the above problems.

SUMMARY OF THE INVENTION

[0008] One objective of the present invention is to provide a leadframe for leadless semiconductor packages. The present leadframe comprises: a plurality of cavities and a plurality of longitudinal gates. Each cavity has at least one die pad for supporting at least one die. Each cavity has a plurality of conducting portions for electrical connection to the die or dice on the die pad or pads. The cavities are arranged in a matrix configuration and classified into a plurality of columns and a plurality of rows. The longitudinal gates are situated between the cavities along the columns. Molding material is injected into the cavities along the columns via the longitudinal gates to package the dice in the cavities.

[0009] Therefore, the leadframe of the invention does not have the runner of the conventional leadframe, and can have more space to support more dice. The density of dice accommodated by the present leadframe can be high, and the packaging efficiency can be improved. Besides, the molding material remaining in the runner can be minimized by using the leadframe of the invention so as to decrease the manufacturing cost.

[0010] Another objective of the invention is to provide an encapsulation method for leadless semiconductor packages. The method comprises the steps of: (a) attaching a plurality of dice to die pads in a plurality of cavities of a leadframe, the cavities arranged in a matrix configuration and classified into a plurality of columns and a plurality of rows; (b) electrically connecting the dice on the die pads to a plurality of conducting portions of the leadframe; and (c) longitudinally injecting molding material into the cavities along the

columns via a plurality of longitudinal gates of the leadframe to package the dice in the cavities, the longitudinal gates situated between the cavities along the columns.

[0011] The method of the invention does not need a film to prevent molding flash, and can solve the problem of molding flash remaining on the conducting portions. The method of the invention does not use expensive cutting equipment so as to decrease the cost and to upgrade the efficiency.

BRIEF DESCRIPTION OF THE DRAWINGS

[0012] The present invention is illustrated by way of example and not by way of limitation, in the figures of the accompanying drawings and in which like reference numerals refer to similar elements and in which:

Fig. 1 shows a conventional leadframe for packaging semiconductor devices with leads.

Fig. 2 shows a conventional leadframe for packaging leadless semiconductor devices.

Fig. 3 shows a conventional leadless semiconductor device.

Fig. 4 shows a top-view of a leadframe for leadless semiconductor packages according to the present invention.

Fig. 5 shows a flow chart illustrating an encapsulation method for leadless semiconductor packages according to the present invention.

DETAILED DESCRIPTION OF THE INVENTION

[0013] Reference will now be made in detail to the embodiments of the invention, examples of which are illustrated in the accompanying drawings. While the invention will be described in conjunction with these embodiments, it will be understood that they are not intended to limit the invention to these embodiments. On the contrary, the invention is intended to cover alternatives, modifications and equivalents, which may be included within the scope of the invention as defined by the appended claims. Furthermore, in the following detailed description of the present invention, numerous specific details are set forth in order to provide a thorough understanding of the present invention. However, it is understood that the present invention may be practiced without these specific details. In other instances, well-known methods, procedures, components, and circuits have not been described in detail as not to unnecessarily obscure aspects of the present invention.

[0014] Referring to Fig. 4, according to the invention, a leadframe 4 for leadless semiconductor packages comprises a plurality of cavities 41, 42, 43, 44, 45, 51, 52, 53, 54, 55 and a plurality of inter-cavity longitudinal gates 46, 47, 48, 49, 56, 57, 58, 59. Each cavity has a die pad (not shown in the figure) for supporting a die. Die 411 is, for example, attached to its die pad in cavity 41. Each cavity has a plurality of conducting portions for electrical connection to the die on the die pad. For example, the cavity 41 has three conducting portions 412, 413 and 414. In the embodiment of the invention illustrated in Fig. 4, each cavity has one die pad for supporting a die. To improve the efficiency, each cavity can have a plurality of die pads for supporting a plurality of dice.

[0015] The cavities are arranged in a matrix configuration, and are classified into a plurality of columns and a plurality of rows. For example, the cavities 41, 42, 43, 44 and 45 form a first column, and the cavities 51, 52, 53, 54 and 55 form a second column. The cavities along the direction of cavities 41 and 51 form a first row, and the cavities along the direction of cavities 42 and 52 form a second row.

[0016] The inter-cavity longitudinal gates 46, 47, 48, 49, 56, 57, 58 and 59 are situated between the cavities along the columns. For example, the longitudinal gate 46 is situated between cavity 41 and cavity 42 for connecting the cavity 41 and the cavity 42. Similarly, the longitudinal gate 47 is situated between the cavity 42 and the cavity 43 for connecting the cavity 42 and the cavity 43. Therefore, the cavities 41, 42, 43, 44 and 45 are connected by the longitudinal gates 46, 47, 48 and 49. Similarly, the cavities 51, 52, 53, 54 and 55 are connected by the longitudinal gates 56, 57, 58 and 59.

[0017] Molding material is injected into the cavities along the columns of the leadframe 4 via the longitudinal gates to package the dice in the cavities. For example, firstly the molding material is injected into a first longitudinal gate 40 of the first column, and then flows into the cavity 41 of the first column via the first longitudinal gate 40. In sequence, the molding material flows into the longitudinal gate 46, the cavity 42, the longitudinal gate 47, the cavity 43, the longitudinal gate 48, the cavity 44, the longitudinal gate 49, and the cavity 45 to package the dice in the cavities along the first column.

[0018] The leadframe 4 of the invention does not have the runner 12 as shown in the conventional leadframe 1 of Fig. 1, and the leadframe 4 can have more space to support more dice. The density of dice accommodated by the leadframe 4 can be high, and the packaging efficiency can be improved. Besides, the molding material left in the runner can be minimized by using the leadframe 4 of the invention so as to decrease the manufacturing cost.

[0019] According to the embodiment of the invention, to further improve the packaging quality, the leadframe 4 further comprises a plurality of transverse (or horizontal) gates 61, 62, 63, 64 and 65. The transverse gates are situated between the cavities along the rows. For example, the horizontal gate 61 is situated between the cavity 41 and the cavity 51 for connecting the cavity 41 and the cavity 51. Similarly, the transverse gate 62 is situated between the cavity 42 and the cavity 52 for connecting the cavity 42 and the cavity 52. When the molding material is injected into the cavities along the columns, the molding material can flow into the transverse gates so as to balance the pressure between the cavities along the rows. The bubbles induced in the cavities by the molding material can be drained by the transverse gates to further improve the packaging quality.

[0020] Referring to Fig. 5, the flow chart illustrates an encapsulation method for semiconductor packages according to the present invention. In step 501, the dice are attached to the die pads in the cavities of the leadframe 4. The leadframe 4 has a plurality of cavities arranged in a matrix configuration and classified into a plurality of columns and a

plurality of rows. In step 502, the dice are electrically connected to the conducting portions of the leadframe 4.

[0021] In step 503, the molding material is injected longitudinally to package the dice. The molding material is injected into the cavities along the columns via the longitudinal gates to package the dice in the cavities along the columns. The longitudinal gates are situated between the cavities along the columns.

[0022] In step 503, the molding material can flow into the transverse gates so as to balance the pressure between the cavities along the rows and to drain the bubbles induced in the cavities by the molding material. The transverse gates are situated between the cavities along the rows.

[0023] The method of the invention does not need a film to prevent flash, and can solve the problem of molding flash remaining on the conducting portions. The method of the invention does not use expensive cutting equipment so as to decrease the cost and to upgrade the efficiency.

[0024] The foregoing descriptions of specific embodiments of the present invention have been presented for purposes of illustration and description. They are not intended to be exhaustive or to limit the invention to the precise forms disclosed, and obviously many modifications and variations are possible in light of the above teaching. The embodiments were chosen and described in order to best explain the principles of the invention and its

practical application, to thereby enable others skilled in the art to best utilize the invention and various embodiments with various modifications as are suited to the particular use contemplated. It is intended that the scope of the invention be defined by the Claims appended hereto and their equivalents.